IN THE SPECIFICATION

Please amend the paragraph beginning on Page 8, line 7 as follows:

--FIG. 4 shows an exemplary local DC voltage generator 230 including NAND gate G1, FET devices F1-3, Capacitor C1 and regulator system 412. PCS(x) and CES(x) are received by G1 which outputs control signal CS(x) for controlling FET F3, preferably a pFET ~~an nFET~~, which switches the regulator system 412 on or off. When either of PCS(x) and CES(x) are "low", CS(x) switches FET F3 "off" so that no DC current flows to the regulator system 412. When both PCS(x) and CES(x) are "high" , CS(x) switches FET F3 "on" and a voltage having a level equal to V_H minus threshold drops of FET devices F1 and F2 is provided to the regulator system 412. FET devices F1, F2, which are preferably pFET devices, are cascade transistors functioning as a voltage divider, where the amount of voltage passing through the FET devices F1, F2 is determined by the size of the FET devices F1, F2 (in a way similar to relatively bulky resistors). Preferably, the FET devices F1 and F2 are different sizes. Capacitor C1 is a decoupling capacitor for reducing power supply noise due to wiring inductance along a supply line connecting the power supply to the regulator system 412. Wiring inductance is further minimized by maintaining the supply line to be short.--